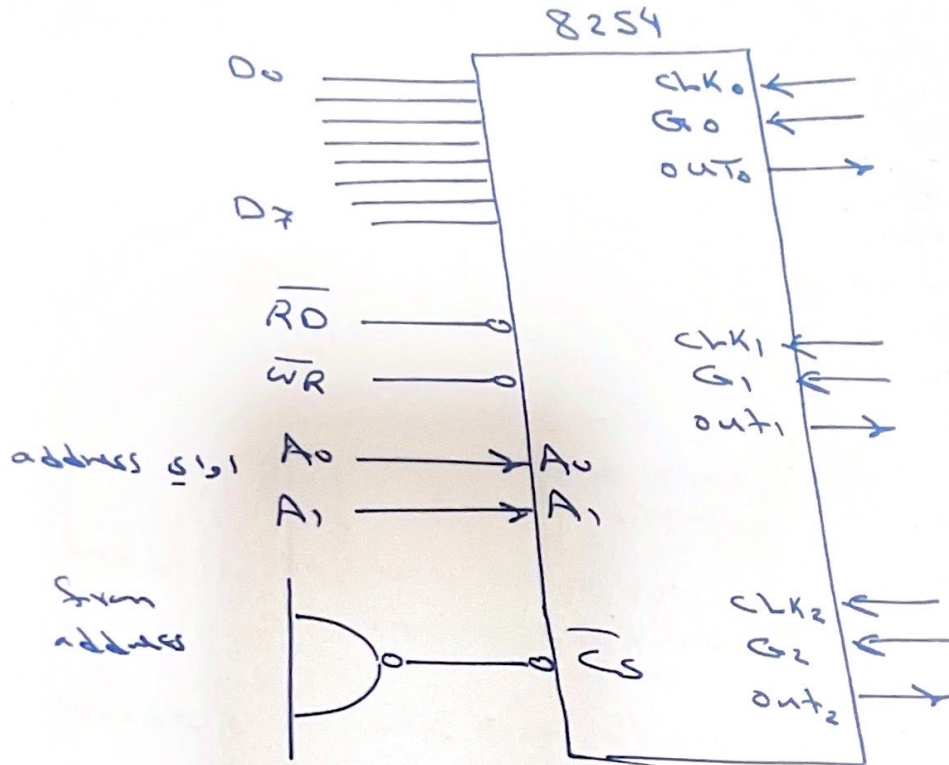


# lecture - 6 -

## Programmable interval timer

8254  
8253

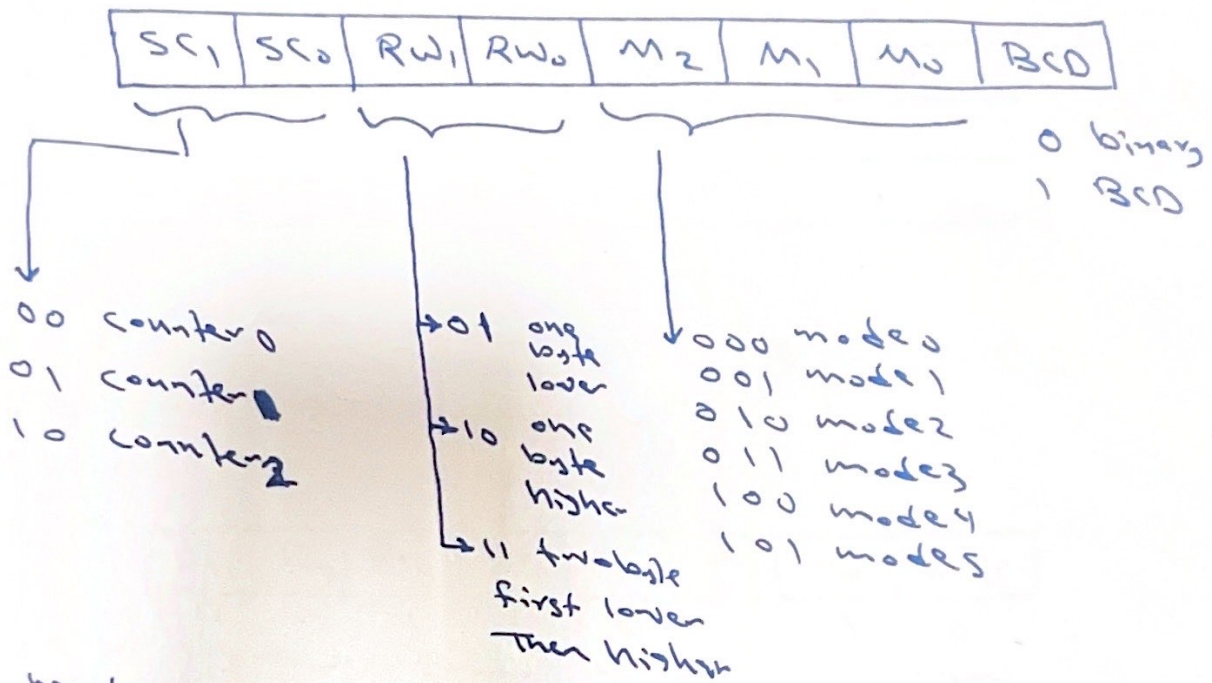
①



|              | A <sub>1</sub> A <sub>0</sub> |
|--------------|-------------------------------|
| Counter 0    | 0 0                           |
| Counter 1    | 0 1                           |
| Counter 2    | 1 0                           |
| Control word | 1 1                           |

## Control Word

(2)



mode 0 event counter  
interrupt on terminal count

mode 2 : Rate generator -  
continuous pulses



mode 3 : Square wave  
rate generator



Ex 5.1  $\overline{CS}$  A7-A2 = 100101

(a) Find port address assign for 8253/8254

(b) Find the configuration 8254 if the control register programmed as follows

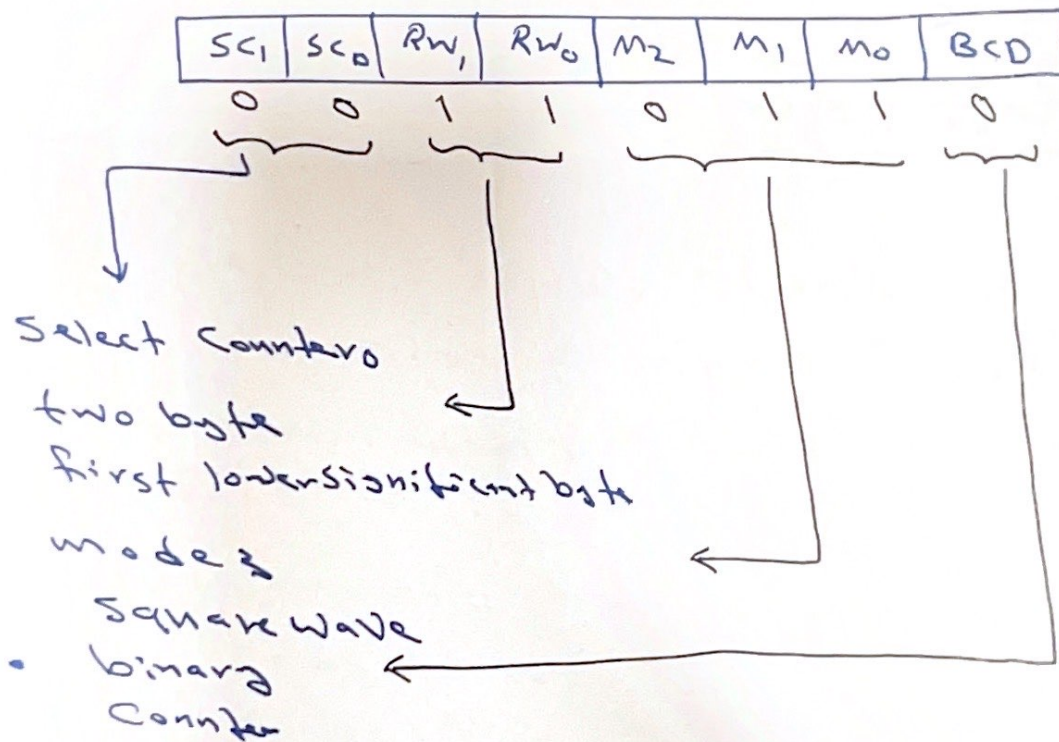
MOV AL, 00110110

OUT 97H, AL

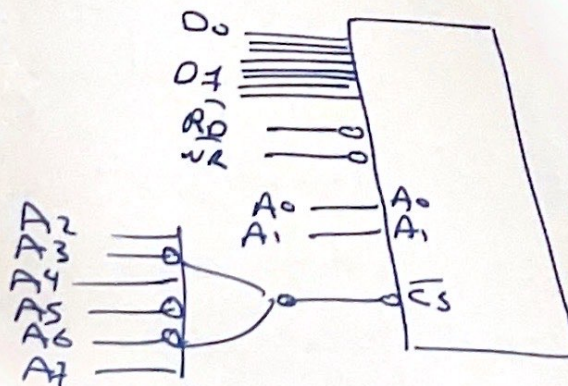
ans = (a)

|              |     | A <sub>7</sub> | A <sub>6</sub> | A <sub>5</sub> | A <sub>4</sub> | A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> |
|--------------|-----|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Counter 0    | 94H | 1              | 0              | 0              | 1              | 0              | 1              | 0              | 0              |
| Counter 1    | 95H | 1              | 0              | 0              | 1              | 0              | 1              | 0              | 1              |
| Counter 1    | 96H | 1              | 0              | 0              | 1              | 0              | 1              | 1              | 0              |
| Control Word | 97H | 1              | 0              | 0              | 1              | 0              | 1              | 1              | 1              |

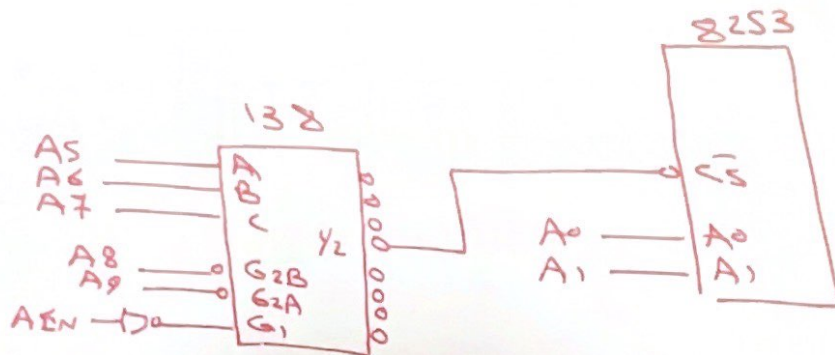
(b) `mov AL, 00110110`  
`out 97H, AL`



note



Ex Find port address & counter address



ans =  $\frac{1}{2} = \begin{matrix} C & B & A \\ 0 & 1 & 0 \\ A_7 & A_6 & A_5 \end{matrix}$

|                  |     | A <sub>9</sub> A <sub>8</sub> | A <sub>7</sub> A <sub>6</sub> | A <sub>5</sub> A <sub>4</sub> | A <sub>3</sub> A <sub>2</sub> A <sub>1</sub> A <sub>0</sub> |
|------------------|-----|-------------------------------|-------------------------------|-------------------------------|-------------------------------------------------------------|
| Counter 0        | 40H | 00                            | 010X                          | XX00                          |                                                             |
| Counter 1        | 41H | 00                            | 010X                          | XX01                          |                                                             |
| Counter 2        | 42H | 00                            | 010X                          | XX10                          |                                                             |
| Control register | 43H | 00                            | 010X                          | XX11                          |                                                             |

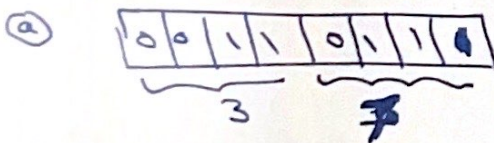
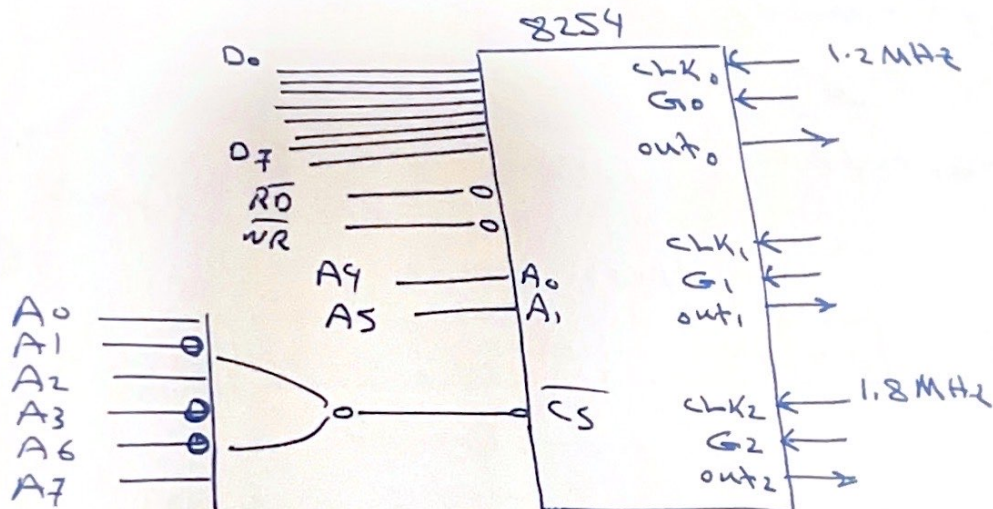
Q Design a timer circuit using 8254 with using counter 0 (B5H) and control using (85H) then write a program

- Counter 0 for binary count of mode 3 to divide clock by 910. (4282)BCD
- Counter 2 for binary count of mode 3 to divide CLK<sub>2</sub> by number C26A Hex
- Find the frequency output from out<sub>0</sub> and out<sub>2</sub> in @ if CLK<sub>0</sub> = 1.2 MHz CLK<sub>2</sub> = 1.8 MHz

ans

(5)

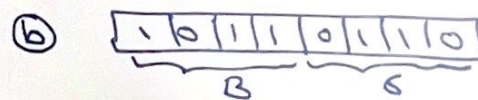
|                  |     | A <sub>7</sub> | A <sub>6</sub> | A <sub>5</sub> | A <sub>4</sub> | A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> |
|------------------|-----|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| counter 0        | B5H | 1              | 0              | 1              | 1              | 0              | 1              | 0              | 1              |
| counter 1        | A5H | 1              | 0              | 1              | 0              | 0              | 1              | 0              | 1              |
| counter 2        | 95H | 1              | 0              | 0              | 1              | 0              | 1              | 0              | 1              |
| Control Register | 85H | 1              | 0              | 0              | 0              | 0              | 1              | 0              | 1              |



```

mov AL, 37H
mov 85H, AL
mov AL, 82H
out 85H, AL
mov AL, 42H
out 85H, AL
HLT

```



```

mov AL, B6H
out 85H, AL
mov AL, 6AH
out 95H, AL
mov AL, C2
out 95H, AL
HLT

```

(c)  $CLK_0 = 1.2M$   $N = 4282$  BCD  $f_{out} = \frac{f_{CLK}}{N} = \frac{1.2 \times 10^6}{4282} = 280Hz$

$CLK_2 = 1.8M$   $N = C26A Hex \rightarrow 49770$

$f_{out} = \frac{f_{CLK}}{N} = \frac{1.8 \times 10^6}{49770} = 36Hz$

Q2 8254 PPI used to generate signal with duty cycle 20%. answer the following

- 1- find the control word for Programming PPI
- 2- find the frequency output if  $GATE_1 = 1$   
 $CLK_1 = 2 MHz$

3- write the required instruction for programming 8254 to generate signal with duty cycle 80% if addressing range 70H-73H

ans

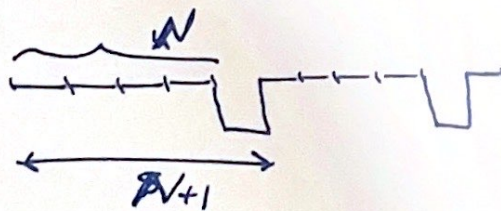
control register

|                 |                 |   |   |                |                |                |     |
|-----------------|-----------------|---|---|----------------|----------------|----------------|-----|
| SC <sub>1</sub> | SC <sub>0</sub> | 0 | 1 | M <sub>2</sub> | M <sub>1</sub> | M <sub>0</sub> | BCD |
|-----------------|-----------------|---|---|----------------|----------------|----------------|-----|

0 1  
counter

0 1 0 0  
mode 2  
continuous pulse  $\neq 50\%$

80% duty cycle



or  
Duty cycle =  $\frac{N}{N+1} = 80\%$

$$\frac{N}{N+1} = 0.8$$

$$N = 0.8N + 0.8$$

$$N - 0.8N = 0.8$$

$$0.2N = 0.8$$

$$N = \frac{0.8}{0.2} = 4$$

$\therefore$  only one byte

$\therefore$  ① control word

0101 0100  
5 4

$\therefore$  control word = 54H

②  $f_{out} = \frac{CLK}{N} = \frac{2M}{4} = 0.5MHz$   
 $= 500kHz.$

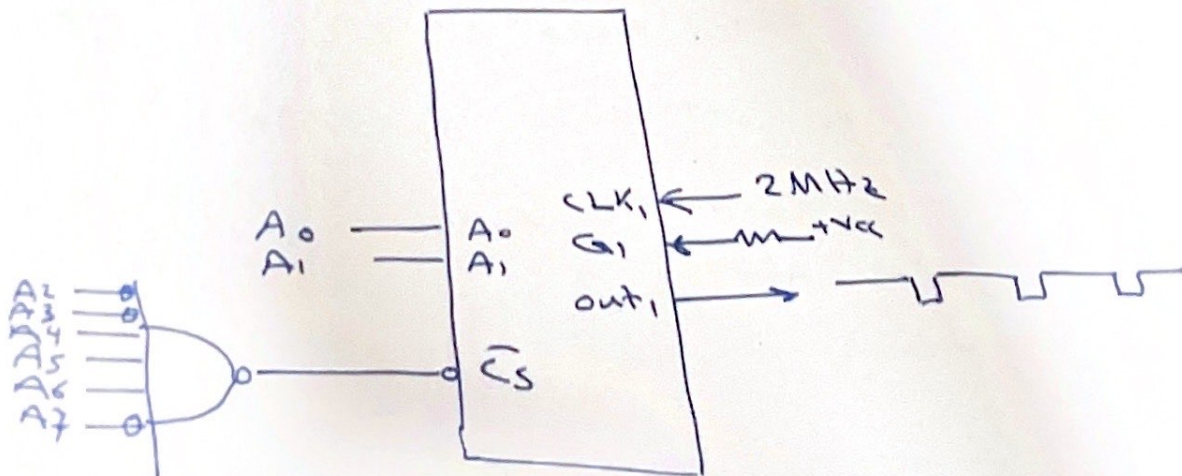
③

Counter 0      70H  
 Counter 1      71H  
 Counter 2      72H  
 Control register 73H

MOV AL, 54H  
 OUT 73H, AL  
 MOV AL, 04  
 OUT 71H, AL  
 HLT

if Design

|    | A <sub>7</sub> A <sub>6</sub> A <sub>5</sub> A <sub>4</sub> | A <sub>3</sub> A <sub>2</sub> A <sub>1</sub> A <sub>0</sub> |
|----|-------------------------------------------------------------|-------------------------------------------------------------|
| 70 | 0 1 1 1                                                     | 0 0 0 0                                                     |
| 71 | 0 1 1 1                                                     | 0 0 0 1                                                     |
| 72 | 0 1 1 1                                                     | 0 0 1 0                                                     |
| 73 | 0 1 1 1                                                     | 0 0 1 1                                                     |

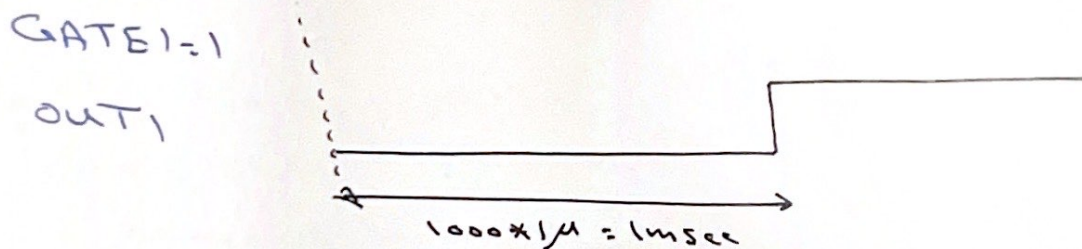


S-7  
Ex assume  $GATE1=1$   $CLK=1MHz$   
 Count  $N=1000$ . Show the output of  
 out<sub>1</sub> if the it is programmed mode 0

ans  
 $\therefore$  mode 0

$$\therefore T = \frac{1}{f} = \frac{1}{1M} = 1\mu sec$$

$\therefore$  output Low for  $NT = 1000 \times 1\mu = 1000\mu sec$   
 $= 1msec$   
 and then remain high

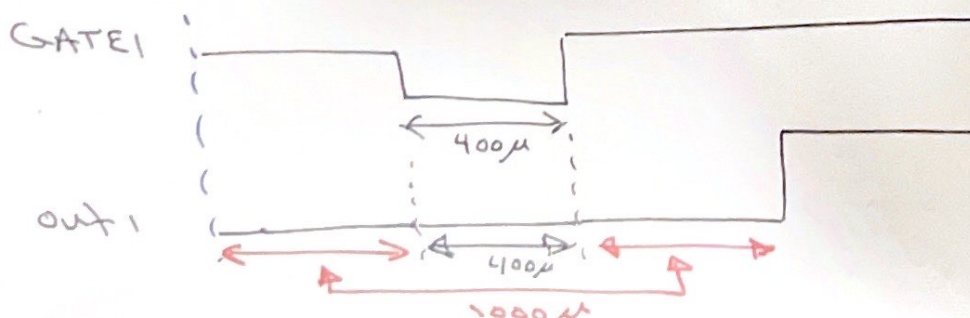


Ex assume  $GATE1$  becomes zero for  $400\mu s$   
 what is the width of the low pulses for  
 out<sub>1</sub> in Ex 5-7

ans  $\therefore NT = 1000 \times 1\mu = 1000\mu sec$

$\therefore GATE1=0$   $400\mu sec$

$\therefore$  low output  $\therefore 1000\mu + 400\mu sec$   
 $= 1400\mu sec$



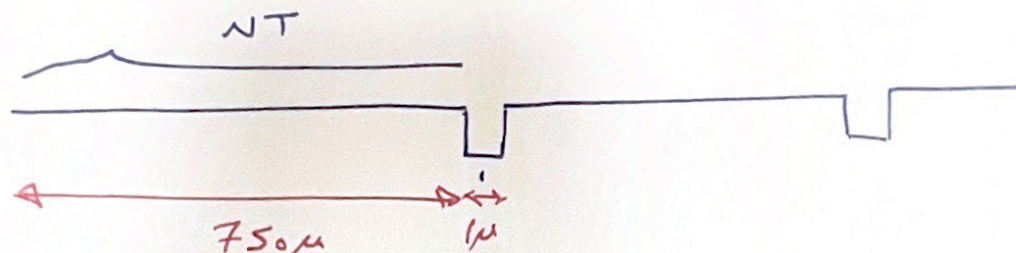
9

Ex 5-10 if  $CLK_2 = 1\text{MHz}$   $GATE_2 = 1$

and  $N = 750$  show out<sub>2</sub> if count<sub>2</sub> is programmed for mod 2

ans  $T = \frac{1}{CLK} = \frac{1}{1\text{M}} = 1\mu\text{sec}$

mode 2



Ex if  $CLK_2 = 1\text{MHz}$   $GATE_1 = 1$

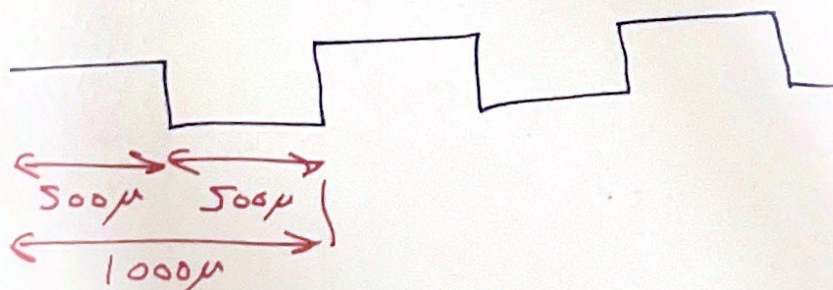
$N = 1000$  show out<sub>1</sub> if count<sub>1</sub> is

Programmed for mode 3

ans  $\therefore$  square wave high = low =  $\frac{N}{2} = 500$

$T = \frac{1}{1\text{M}} = 1\mu\text{sec}$

$\frac{N}{2} T = \frac{1000}{2} \times 1\mu = 500\mu\text{sec}$



Ex if  $CLK_2 = 1\text{MHz}$   $GATE_1 = 1$

$N = 19$

ans high =  $\frac{N+1}{2} = \frac{19+1}{2} = \frac{20}{2} = 10$

low =  $\frac{N-1}{2} = \frac{19-1}{2} = \frac{18}{2} = 9$

